

~~【書類名】 図面~~

~~【図1】~~

~~従来技術~~

Prior Art

Fig. 1

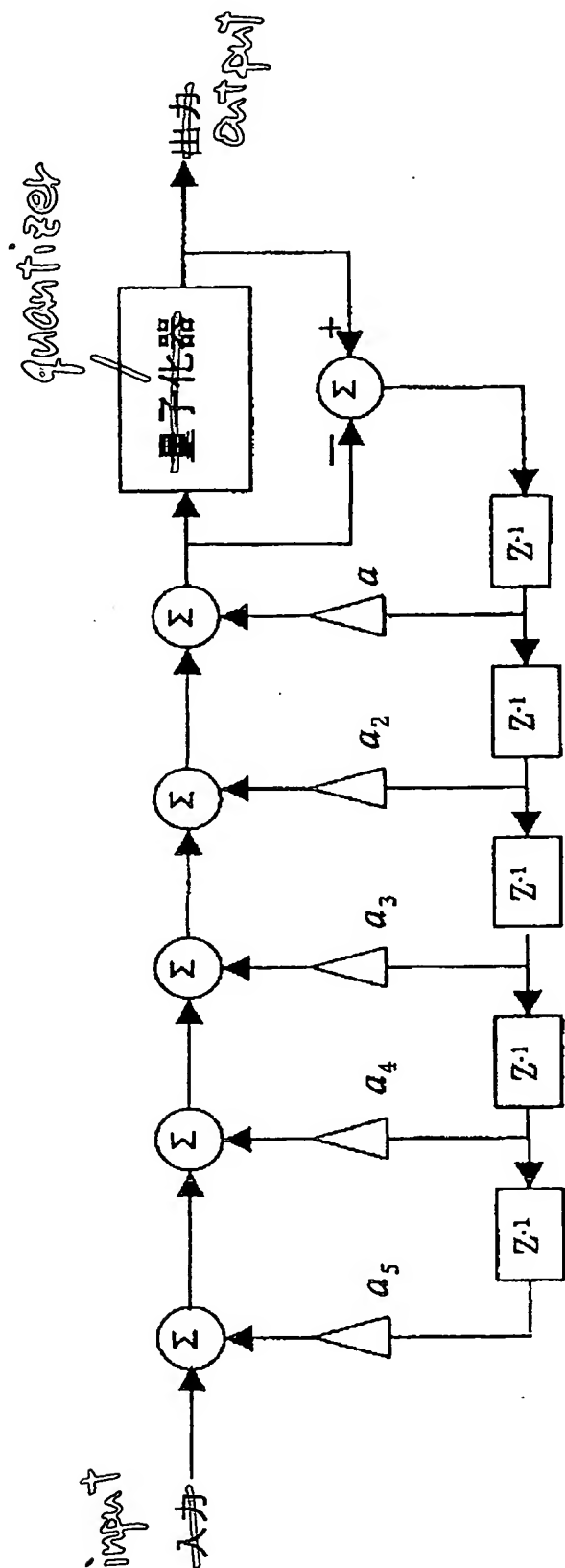


図2

Fig. 2

~~従来技術~~

Prior Art

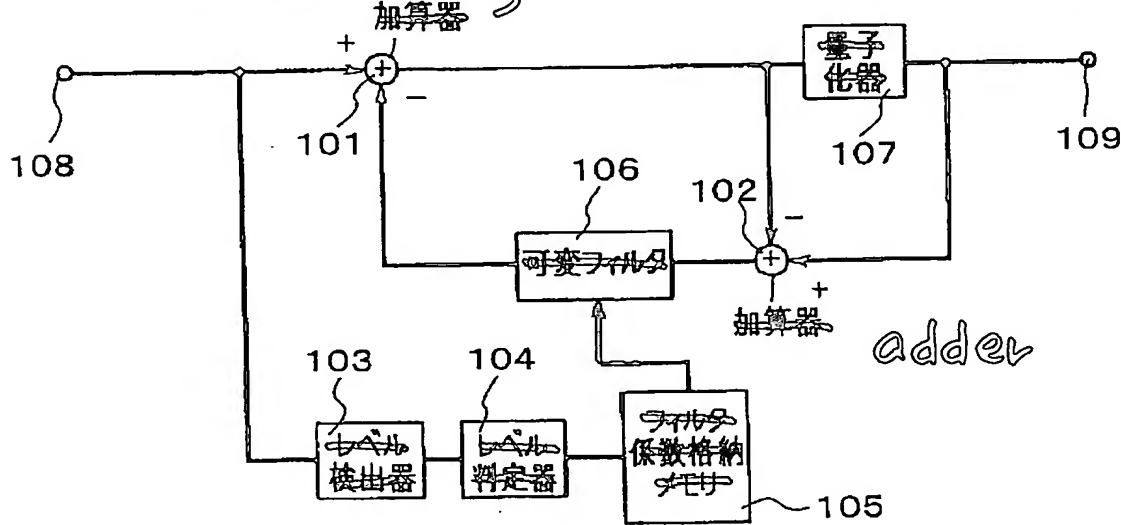
m-bit signal input terminal

n-bit signal (output terminal)

~~m-bit 信号入力端子~~

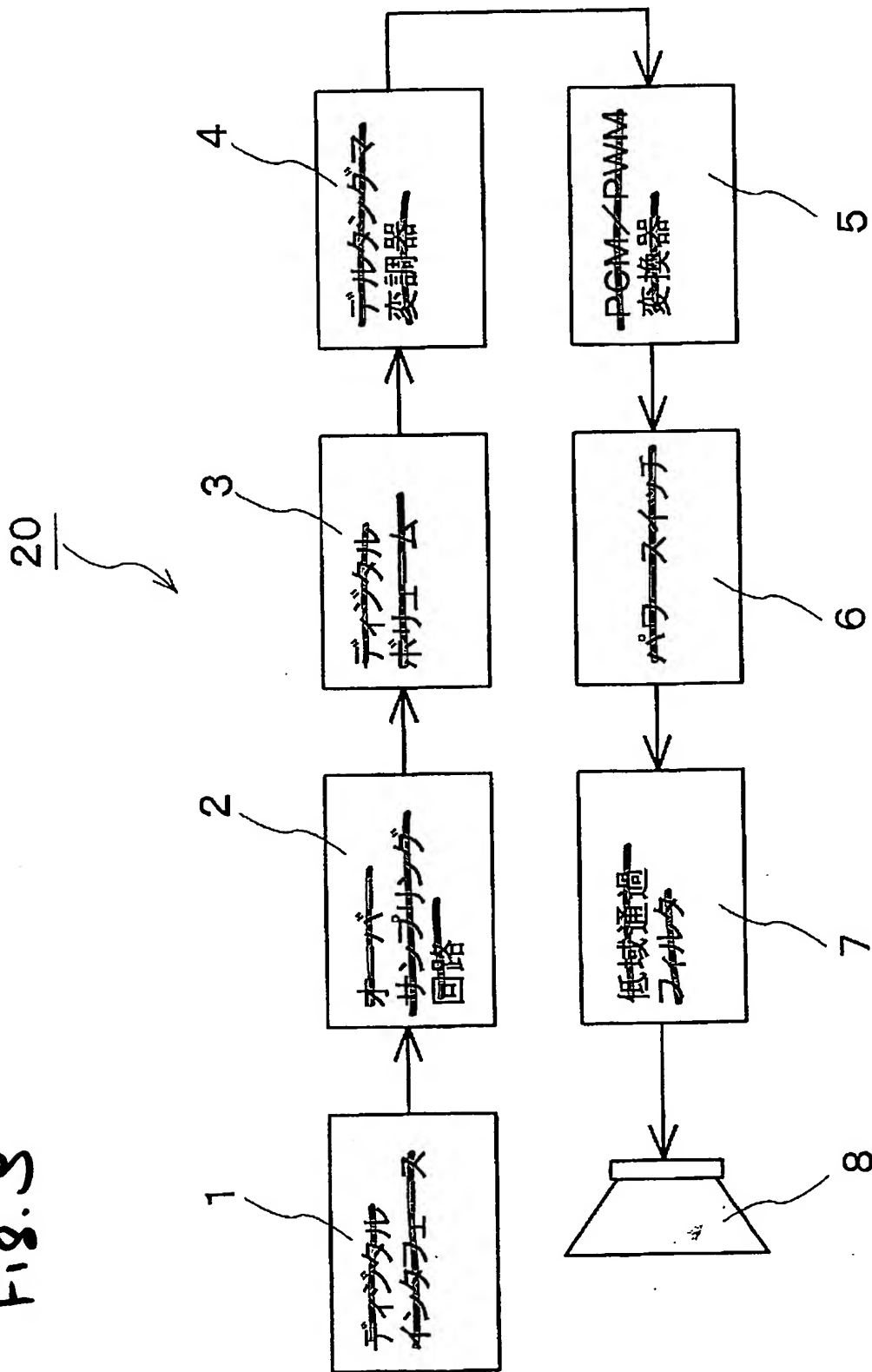
adder

~~n-bit 信号出力端子~~



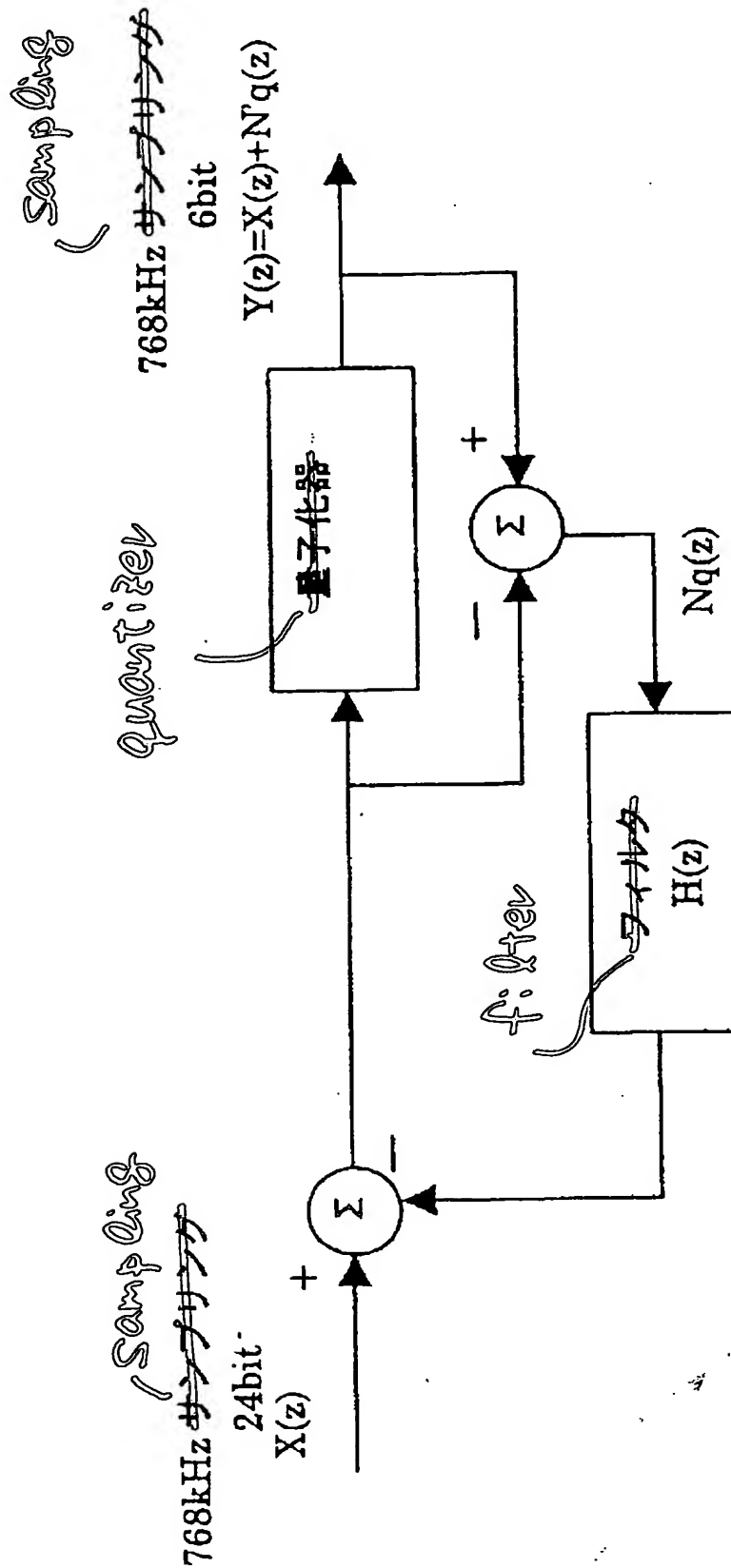
【図 8】

Fig. 3



〔図4〕

Fig. 4



【図5】

coefficient bits

係数ビット: 24

Fig. 5

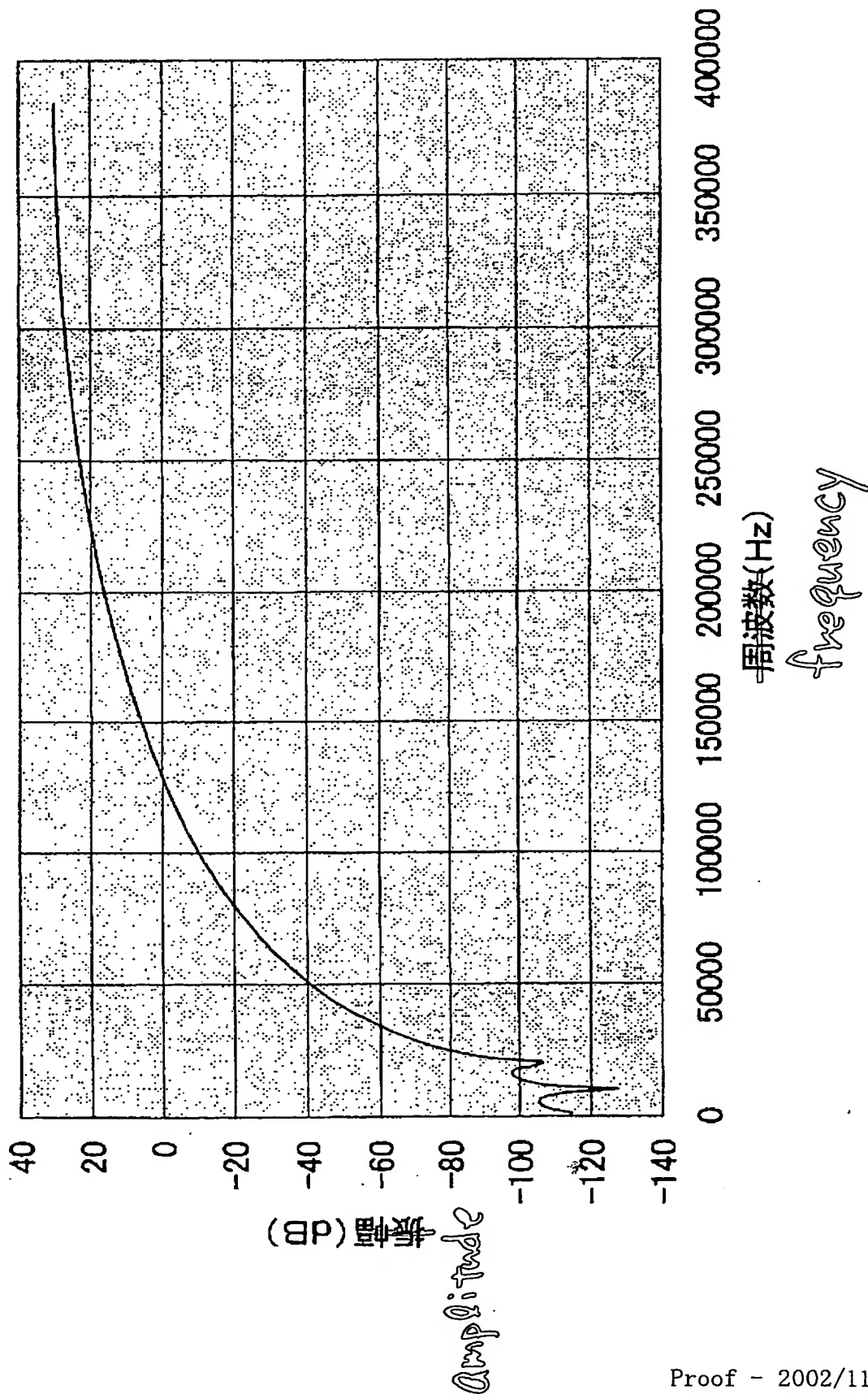


図6

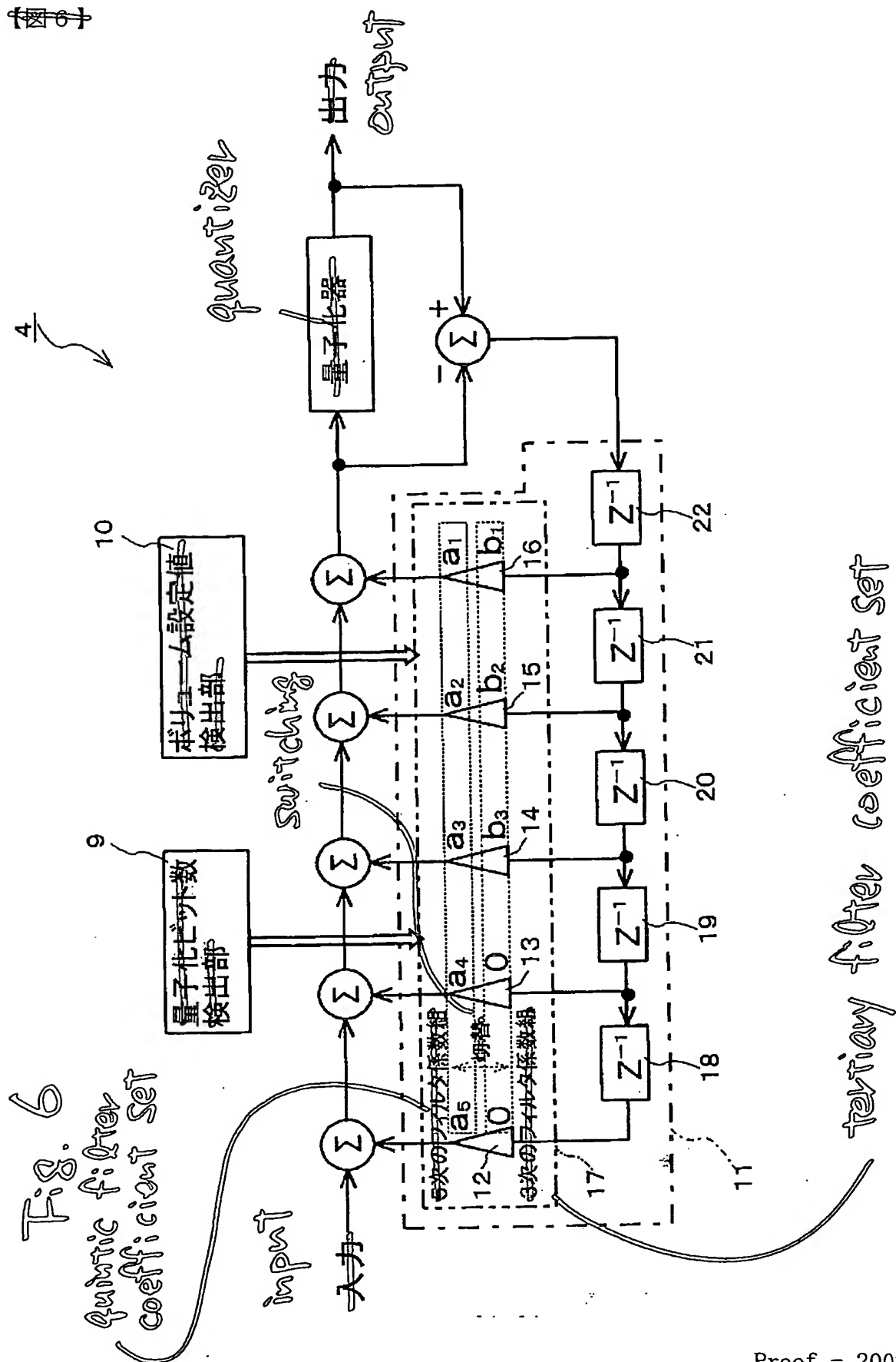


Fig. 7

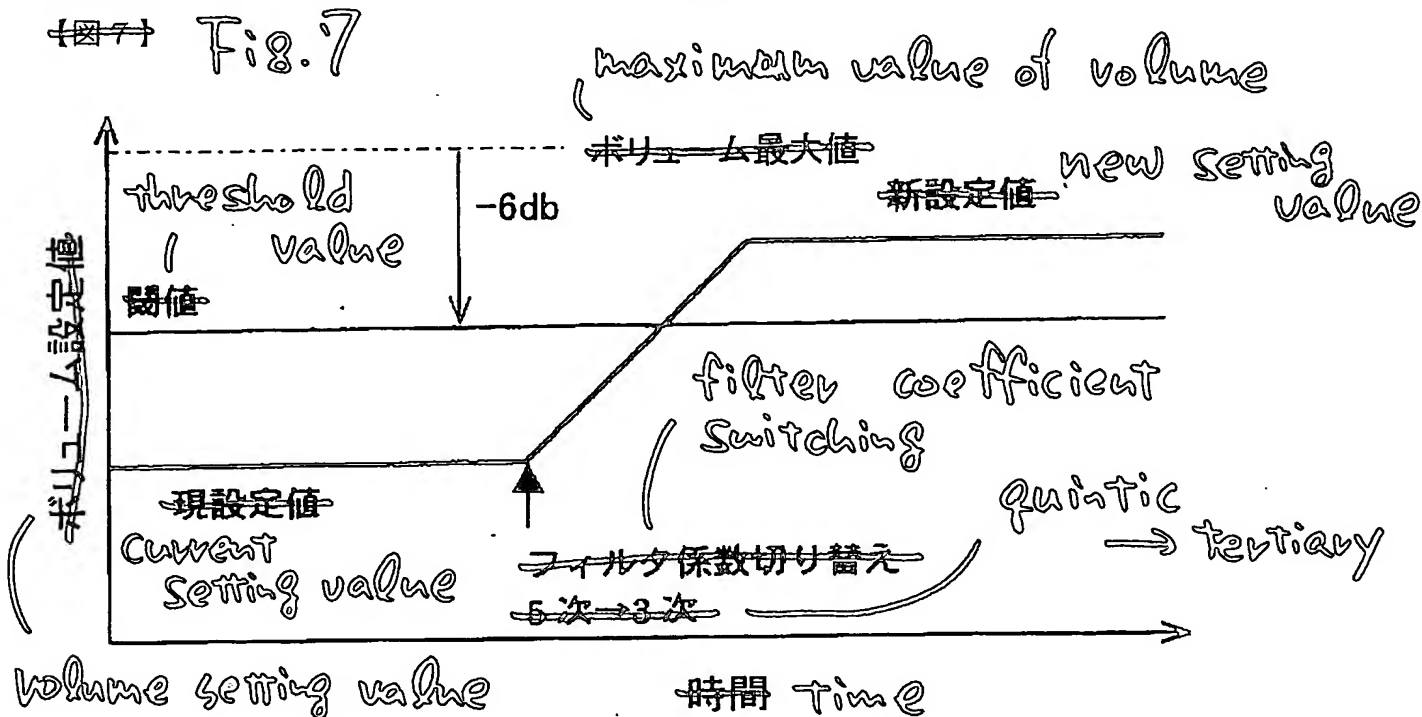
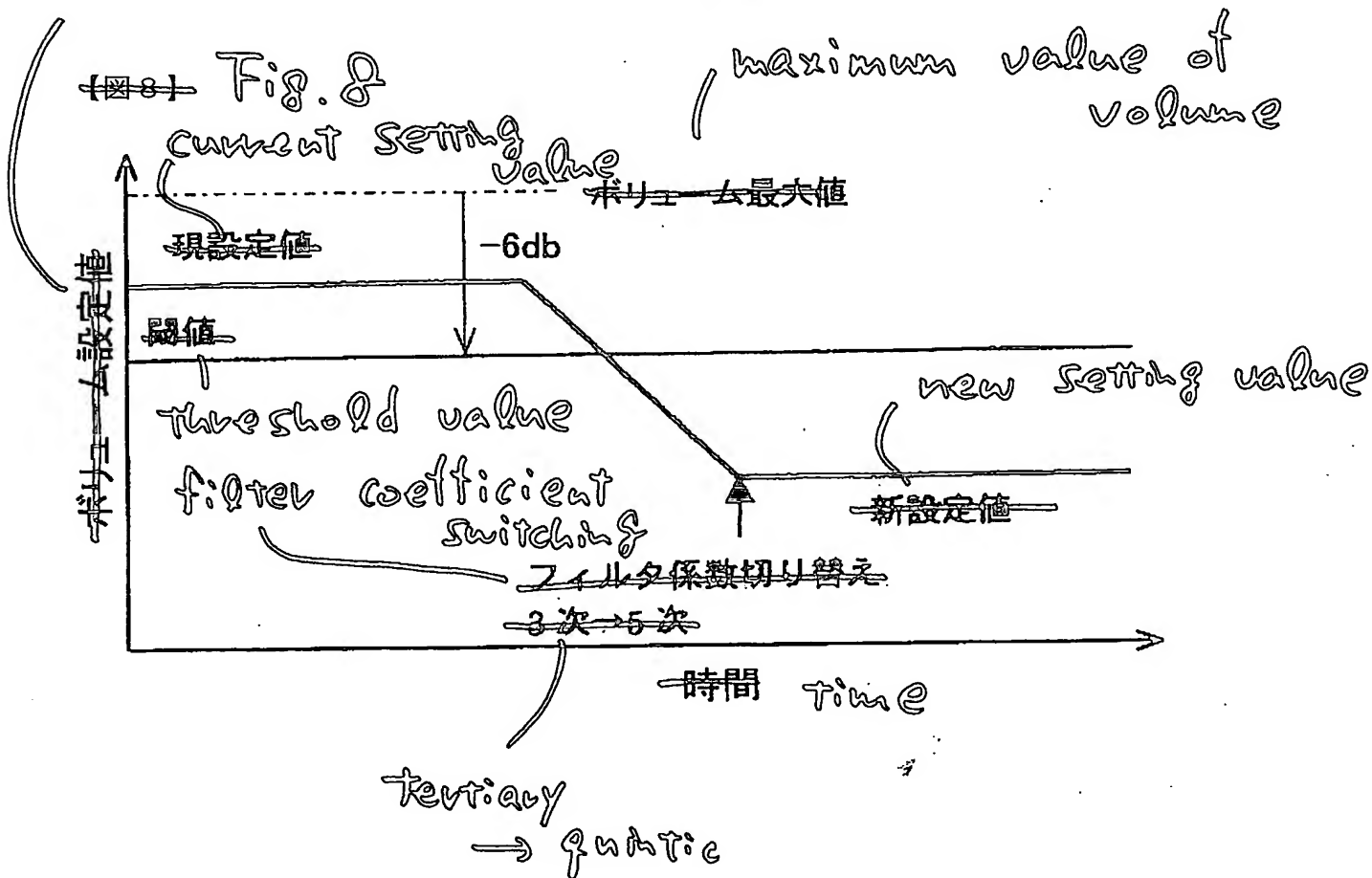
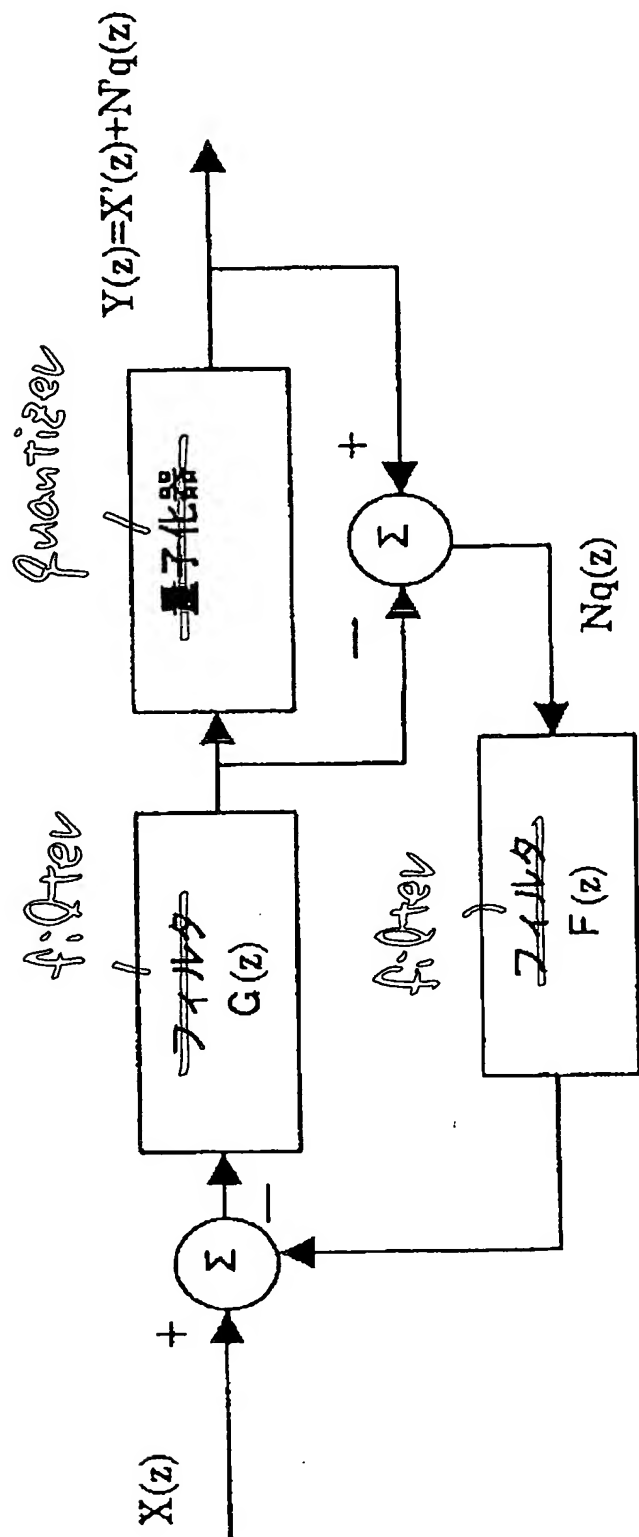


Fig. 8



〔図9〕

Fig. 9

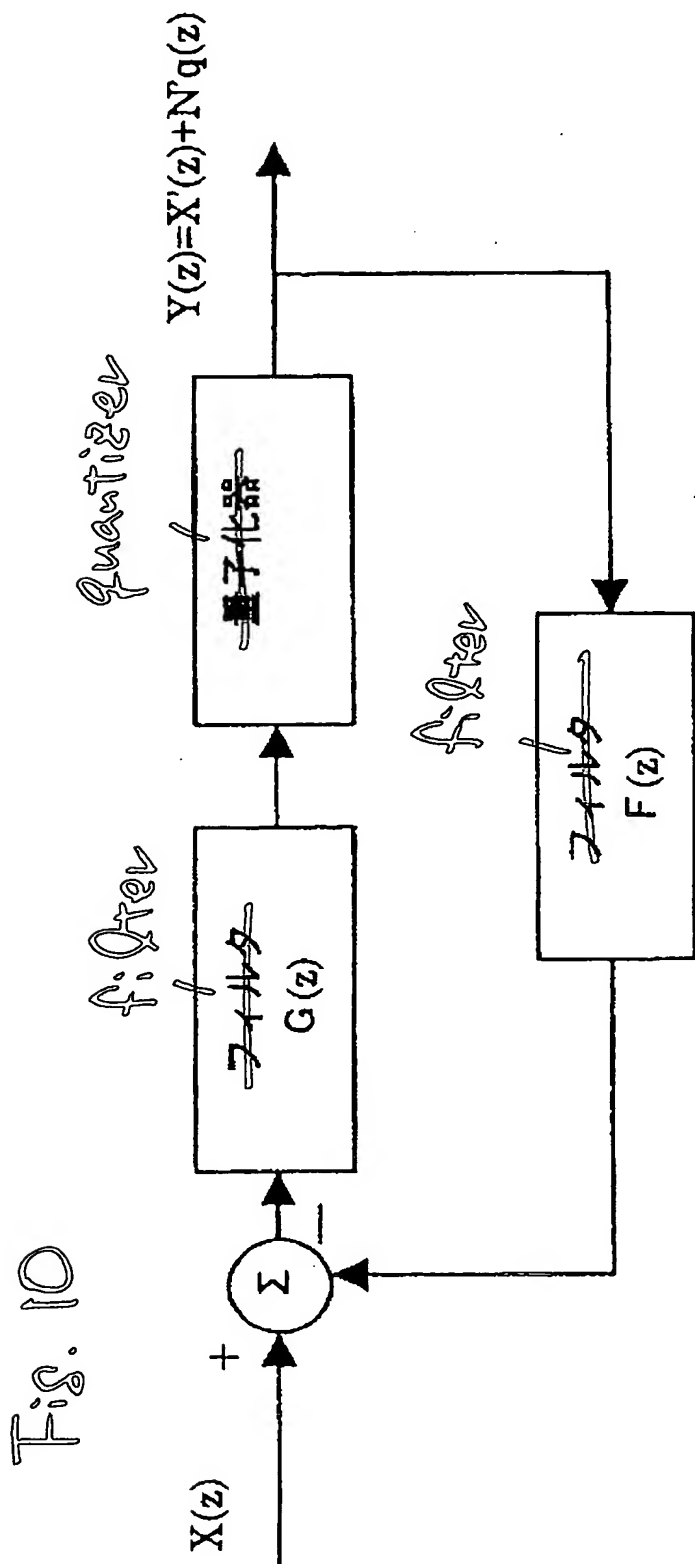


$$X'(z) = G(z)X(z)$$

$$N'q(z) = (1 - F(z)G(z))Nq(z)$$



【図10】



$$X'(z) = \frac{G(z)}{1 + F(z)G(z)} X(z)$$

$$N'q(z) = \frac{1}{1 + F(z)G(z)} Nq(z)$$